WHAT IS CLAIMED IS:

1. A method of forming a memory, the method comprising:

providing a substrate having a non-volatile memory region and a volatile memory region;

forming bottom electrodes of storage capacitors in the volatile memory region;

forming a first dielectric layer on the substrate;

forming a first polysilicon layer on the first dielectric layer;

forming a poly-oxide layer of a split-gate transistor in the non-volatile memory region;

etching the first polysilicon layer to form a floating gate of a split-gate transistor;

forming a top electrode of a capacitor; and

forming a control gate of the split-gate transistor.

2. The method of claim 1 wherein the step of forming bottom electrodes is performed by:

patterning a mask to expose portions of the substrate where the storage capacitors are to be located; and

implanting the exposed portions of the substrate.

3. The method of claim 2 wherein the mask includes a pad oxide layer.

4. The method of claim 2 wherein the mask includes a silicon nitride layer.

5. The method of claim 1 wherein the step of forming the poly-oxide is performed by:

forming a second mask on the first polysilicon layer;

patterning the second mask to expose portions of the first polysilicon layer; and

oxidizing the exposed portions of the first polysilicon layer.

6. The method of claim 5 wherein the second mask is a hard mask comprising silicon nitride.

7. The method of claim 6 wherein the step of patterning the second mask includes etching the second mask using a dry plasma etch process.

8. The method of claim 1 wherein the steps of etching the first polysilicon layer to form a floating gate and forming the top electrode are performed in the same process step.

9. The method of claim 1 wherein the steps of forming the control gate and forming the top electrode are performed in the same process step.

10. A method of forming a memory, the method comprising:

providing a substrate;

forming bottom electrodes of a capacitor;

forming a first dielectric layer on the substrate;

forming a first polysilicon layer on the first dielectric layer;

oxidizing a first portion of the first polysilicon layer to form a first poly-oxide layer a split-gate transistor;

oxidizing a second portion of the first polysilicon layer to form a second poly-oxide layer to define a portion of the first polysilicon layer that is to become a top electrode of a capacitor;

etching the first polysilicon layer to form a floating gate of a split-gate transistor and a top electrode of a capacitor; and

forming a control gate of the split-gate transistor.

11. The method of claim 10 wherein the capacitor is formed along the edge of a shallow trench isolation.

12. The method of claim 10 wherein the step of forming bottom electrodes is performed by:

patterning a mask to expose portions of the substrate where the storage capacitors are to be located; and

implanting the exposed portions of the substrate.

13. The method of claim 12 wherein the mask includes a pad oxide layer.

14. The method of claim 12 wherein the mask includes a silicon nitride layer.

15. The method of claim 10 wherein the step of oxidizing the first portion is performed by:

forming a second mask on the first polysilicon layer;

patterning the second mask to expose portions of the first polysilicon layer; and

oxidizing the exposed portions of the first polysilicon layer.

16. The method of claim 15 wherein the second mask is a hard mask comprising silicon nitride.

17. The method of claim 16 wherein the step of patterning the second mask includes etching the second mask using a dry plasma etch process.

18. The method of claim 10 wherein the step of oxidizing the second portion is performed by:

forming a third mask on the first polysilicon layer;

patterning the third mask to expose portions of the first polysilicon layer; and

oxidizing the exposed portions of the first polysilicon layer.

19. The method of claim 18 wherein the third mask is a hard mask comprising silicon nitride.

20. The method of claim 19 wherein the step of patterning the third mask includes etching the third mask using a dry plasma etch process.

21. The method of claim 10 wherein the step of forming a floating gate of a split-gate transistor and a top electrode of a capacitor is performed in the same process step.

22. An integrated circuit comprising:

a volatile memory region including:

a bottom capacitor electrode;

a dielectric layer patterned to form a capacitor dielectric; and

a polysilicon layer patterned to form a top capacitor electrode;

a non-volatile memory region including:

said dielectric layer patterned to form a tunneling gate dielectric of a split-gate transistor;

said polysilicon layer patterned to form a floating gate of the split gate transistor; and

a poly-oxide region formed in said polysilicon layer substantially self-aligned with the floating gate.

23. The integrated circuit of claim 22, wherein the bottom capacitor electrode is formed a portion of a substrate that has been doped.

24. The integrated circuit of claim 22, wherein the bottom capacitor electrode is formed along the edge of a shallow trench isolation.